

FIG. 1(a)

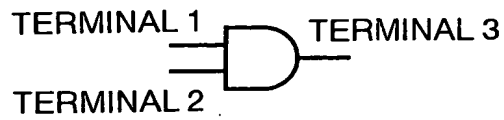


FIG. 1(b)

INPUT PIN	OUTPUT PIN	RISE/FALL OF INPUT	RISE/FALL OF OUTPUT	DELAY TIME (ns)
TERMINAL 1	TERMINAL 3	rise	rise	1
TERMINAL 1	TERMINAL 3	rise	fall	2
TERMINAL 1	TERMINAL 3	fall	rise	3
TERMINAL 1	TERMINAL 3	fall	fall	4
TERMINAL 2	TERMINAL 3	rise	rise	5
TERMINAL 2	TERMINAL 3	rise	fall	6
TERMINAL 2	TERMINAL 3	fall	rise	7
TERMINAL 2	TERMINAL 3	fall	fall	8

FIG. 1(c)

TERMINAL 2 \ TERMINAL 1	0	1
0	0	0
1	0	1

FIG. 2

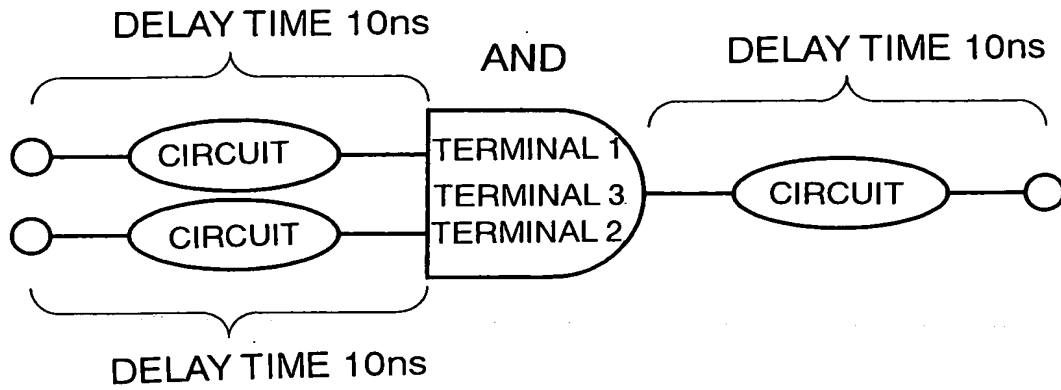


FIG. 3

RISE/FALL OF INPUT	BOTH INPUTS RISE	Rise/fall	BOTH INPUTS FALL
INPUT 1			
INPUT 2			
OUTPUT			
DELAY CAUSED BY: INPUT	INPUT RISING LATER	NONE	INPUT FALLING EARLIER

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FIG. 4

OUTPUT	SELECTED INPUT
R i s e	INPUT RISING LATER
F a l l	INPUT FALLING EARLIER

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FIG. 5

INPUT PIN	OUTPUT PIN	RISE/FALL OF INPUT	RISE/FALL OF OUTPUT	DELAY TIME (ns)
TERMINAL 1	TERMINAL 3	rise	rise	1
TERMINAL 1	TERMINAL 3	rise	fall	2
TERMINAL 1	TERMINAL 3	fall	rise	3
TERMINAL 1	TERMINAL 3	fall	fall	4
TERMINAL 2	TERMINAL 3	rise	rise	5
TERMINAL 2	TERMINAL 3	rise	fall	6
TERMINAL 2	TERMINAL 3	fall	rise	7
TERMINAL 2	TERMINAL 3	fall	fall	8

OUTPUT RISES

OUTPUT FALLS

FIG. 6

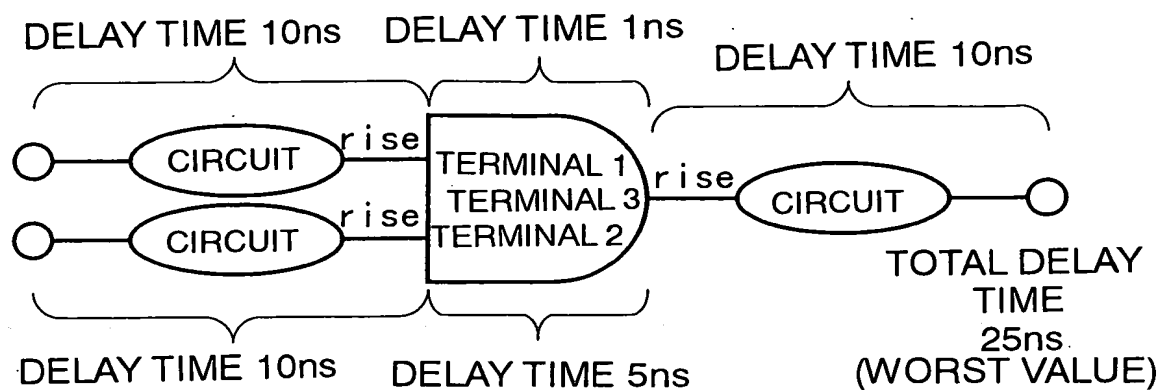
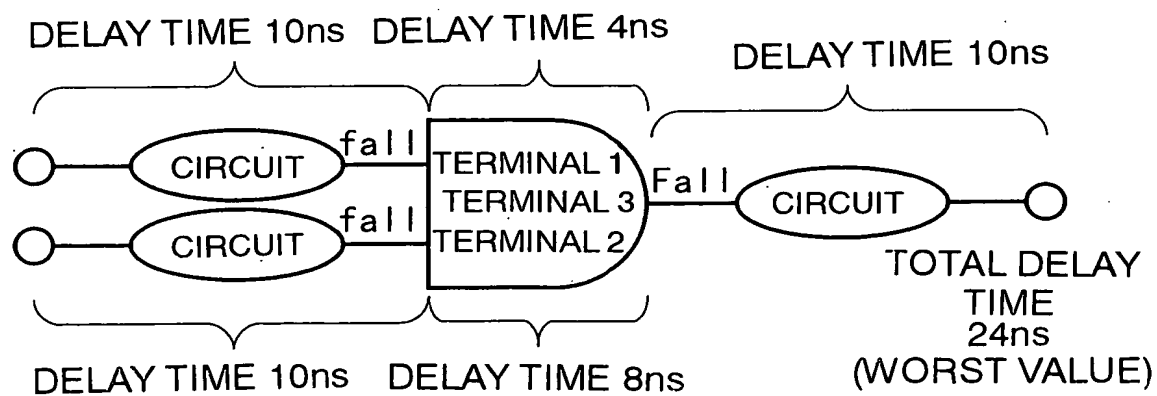


FIG. 7



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